REMARKS

Claims 1-10, 13 and 14 are pending in this application. Claims 11 and 12 have been canceled. Claims 13 and 14 have been newly added. Claim 9 is herein amended. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Drawings

The drawings were objected to because there is no Fig. 10F or Fig. 10G. Attached is a copy of Figs. 10F and 10G with our stamped postcard filing receipt as evidence that these Figures were filed.

Rejections under 35 USC §112, Second Paragraph

Claims 9 and 10 were rejected under 35 USC §112, second paragraph, as being indefinite.

The step at lines 23-26 of claim 9 referred to by the examiner has been amended as follows:

> etching the ~~third~~ second film by using the partially etched third film as a mask to form a via hole reaching the first film in an area where the second opening is formed, and to form a wiring groove to an intermediate depth of the second film in an area where the first opening is formed and the second opening is not formed

It is believed that the amended claims are in full compliance with 35 USC§112.

Rejections under 35 USC §102(b)

Claim 1 was rejected under 35 USC §102(b) as being anticipated by Olsen (EP 0 926 715).

In so doing, the Examiner asserted as follows:

> Olsen discloses a fabrication method for an integrated circuit. An oxide layer and/or a thin dielectric layer, such as silicon nitride (applicant's first film being made of a material having a different etch resistance from SiC), is formed on a semiconductor wafer. This is followed by the deposition of a silicon carbide layer (applicant's second film). The silicon carbide layer is deposited using hydrogen containing sources gases, such as silane/methane or trimethylsilane, and is therefore hydrogenated. A photoresisit is deposited and patterned. The silicon carbide and other underlying layers are etched [00115]-[0016]. . . . .

Olsen describes at [0016] as follows:

> Following the SiC deposition, **photoresist is deposited and patterned to expose areas where isolation structures are desired**, giving the structure shown in Figure 2A. **The silicon carbide, optional nitride, oxide and silicon are etched (step 130) to form trenches 90.** A thin layer of oxide will typically be grown on the walls of the trench, . . .

In Olsen, the silicon carbide, optional nitride, oxide and silicon are etched at the same time using the photoresist as a mask. In Olsen, the optional nitride and oxide, which allegedly correspond to "first layer" are etched by using the photoresist but not the silicon carbide as a mask. Thus, Olsen does not teach or suggest "etching the first film by using the second film as a mask."

For at least these reasons, claim 1 patentably distinguishes over Olsen.

Rejections under 35 USC §103(a)

Claims 2, 5, 7 and 9 were rejected under 35 U.S.C. §103(a) as being obvious over Li (US 2002/0177322).

Claim 2 recites, among other things, the step of "**ashing and removing the resist film**" between "etching the second film by using the resist mask as an etching mask to form a recess and expose a partial surface area of the first film on the bottom of the recess" and "dry-etching the first

film exposed on the bottom of the recess by using mixture gas of fluorocarbon gas added with at least one of SF_6 and NF_3 to expose the conductive region of the substrate."

Similarly, claim 7 recites "etching the second film by using the resist mask as an etching mask under a condition that an etching rate of the second film is faster than an etching rate of the first film, to form a recess and expose a partial surface area of the first film on a bottom of the recess; **ashing and removing the resist film**; and dry-etching the first film exposed on the bottom of the recess by using mixture gas of fluorocarbon gas added with at least one of SF_6 and NF_3, to expose the conductive member of the substrate."

Also, claim 9 recites "etching the third film by using the resist mask as an etching mask and using mixture gas of fluorocarbon gas added with at least one of SF_6 and NF_3 to expose a partial surface of the second film; **removing the first resist film**; forming a second resist film with a second opening on surfaces of the etched third film and exposed second film, the second opening being included in an area of the first opening and partially overlapping with the wiring."

Li et al describes as follows:

> [0045] FIGS. 2A-D show schematics of how a silicon carbide layer can be etched during a trench-first dual-damascene etch process. FIG. 2A shows a pre-etch condition wherein an opening 30 corresponding to a trench is provided in a photoresist masking layer 32 which overlies a stack of layers including a mask layer 33, a first low-k dielectric layer 34, a first stop layer 36 such as silicon nitride or silicon carbide, a second low-k dielectric layer 38, a second stop layer 40 such as silicon nitride or silicon carbide, and a substrate 42 such as a silicon wafer which may further include metallization and barrier layers (not shown) beneath the stop layer 40. FIG. 2B shows the structure after etching wherein the opening 30 extends through the low-k dielectric layer 34 to the first stop layer 36. FIG. 2C shows the structure after re-patterning for a via 44. FIG. 2D shows the structure after etching wherein the second low-k dielectric layer 38 is etched down to the second stop layer 40.

Nothing in Li et al indicates that "**(ashing and) removing the resist film**" is conducted between "etching the second film by using the resist mask as an etching mask to form a recess and expose a partial surface area of the first film on the bottom of the recess" and "dry-etching the first film exposed on the bottom of the recess by using mixture gas of fluorocarbon gas added with at least one of SF_6 and NF_3 to expose the conductive region of the substrate."

For at least these reasons, claims 2, 7 and 9 patentably distinguish over Li et al. Claim 5, depending from claim 2, also patentably distinguishes over Li et al for at least the same reason.

Claims 3 and 4 were rejected under 35 U.S.C. §103(a) as being obvious over Li, and further in view of Bajaj (U.S. Patent No. 6,261,157).

Bajaj has been cited for allegedly disclosing that in a typical semiconductor device the conductive layer is formed by depositing copper, while the barrier layer is formed by depositing tantalum. Such a disclosure, however, does not remedy the deficiencies of Li et al.

For at least these reasons, claims 3 and 4, depending from claim 2, also patentably distinguish over Li et al and Bajaj.

Claims 6, 8 and 10 were rejected under 35 U.S.C. §103(a) as being obvious over Li, and further in view of Dabbaugh et al (U.S. Patent No. 6,362,094).

Dabbaugh et al has been cited for allegedly disclosing semiconductor manufacturing method using hydrogenated silicon carbide and also teaches that hydrogenated silicon carbide layer may be conventionally formed by plasma enhanced CVD using a silane source and an oxygen

source and that tetramethilsilane may be used as the silane source while carbon dioxide layer be used for the oxygen source. Such disclosures, however, do not remedy the deficiencies of Li et al.

For at least these reasons, claims 6, depending from claim 2, claim 8, depending from claim 7, and claim 10, depending from claim 9, also patentably distinguish over Li et al.

Claims 11 and 12 were rejected under 35 U.S.C. §103(a) as being obvious over Li in view of Dabbaugh et al.

This rejection has been rendered moot by cancellation of claims 11 and 12.

Claims 13 and 14, depending from claim 1, have been added reciting recitations of claims 11 and 12.

It is submitted that nothing in the cited references, taken either alone or in combination, teaches or suggests all the features recited in each claim of the present invention. Thus all pending claims are in condition for allowance. Reconsideration of the rejections, withdrawal of the rejections and an early issue of a Notice of Allowance are earnestly solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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Attachments: Figs. 10F and 10G
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